FIG. 1

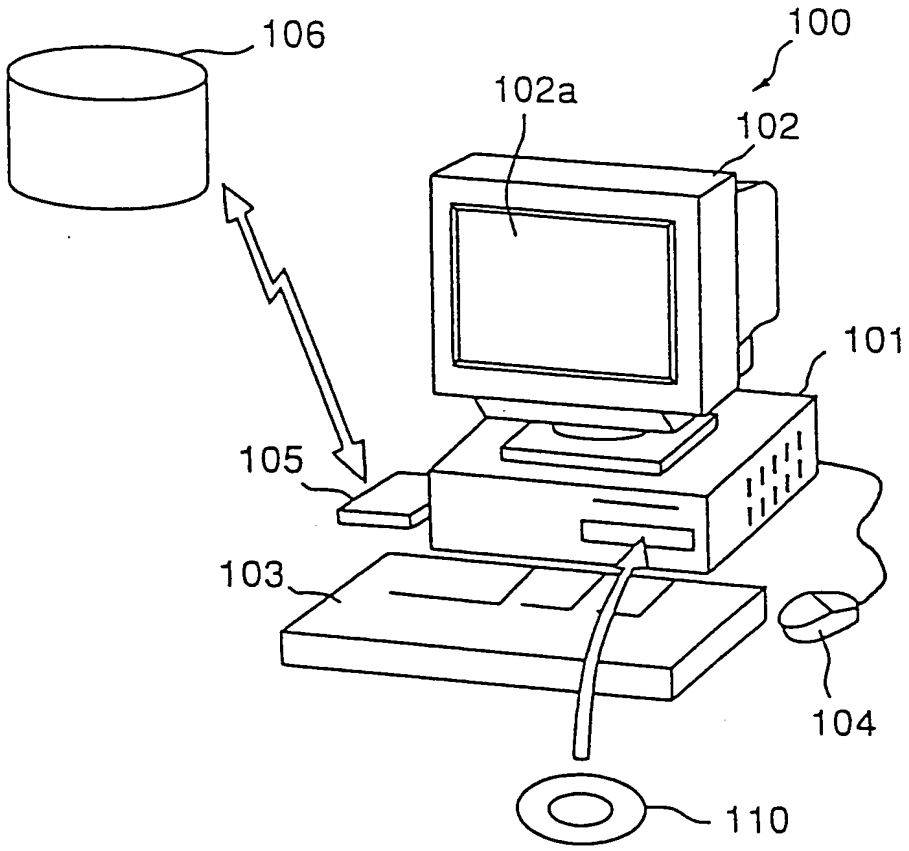

FIG. 2

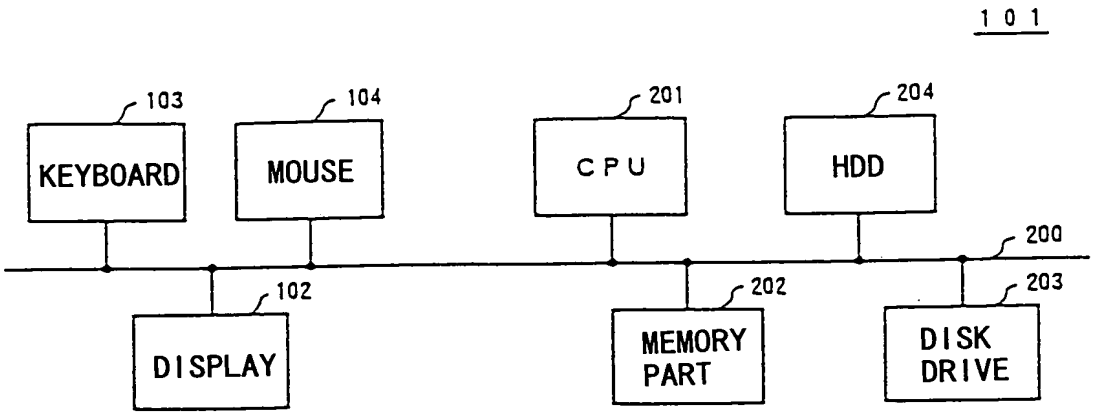
101
103
KEYBOARD
104
MOUSE
201
CPU
204
HDD
200
102
DISPLAY
202
MEMORY PART
203
DISK DRIVE

FIG.3

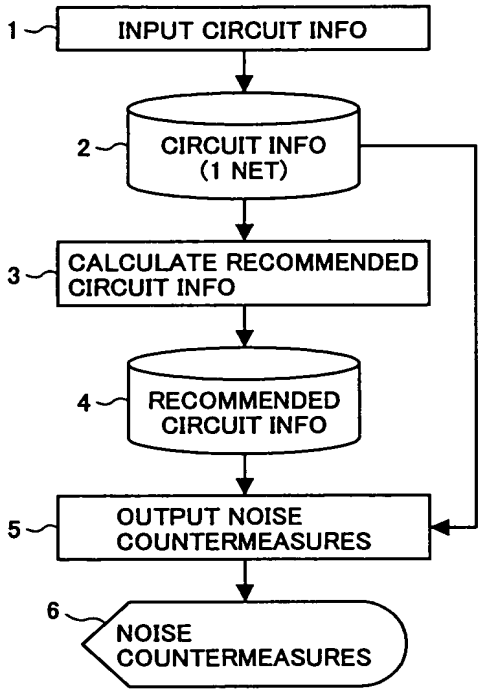
1
INPUT CIRCUIT INFO
2
CIRCUIT INFO
(1 NET)
3
CALCULATE RECOMMENDED
CIRCUIT INFO
4
RECOMMENDED
CIRCUIT INFO
5
OUTPUT NOISE
COUNTERMEASURES
6
NOISE
COUNTERMEASURES

FIG.4

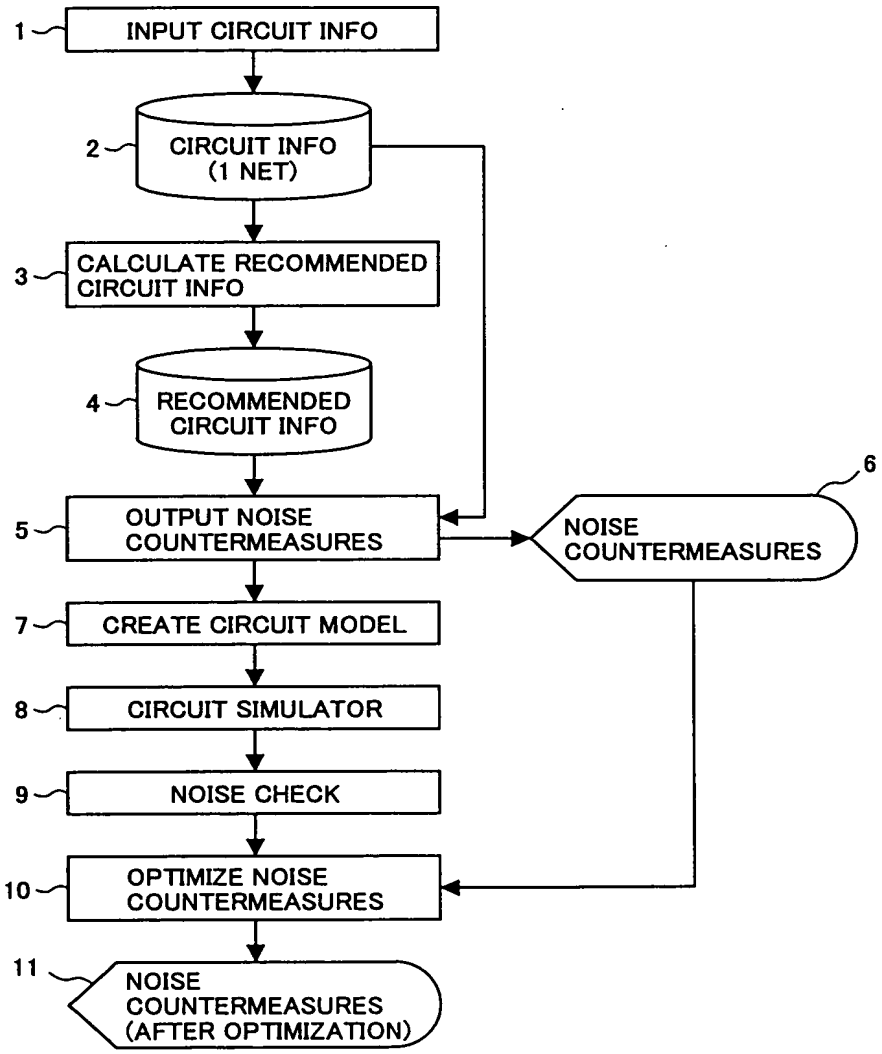
1
INPUT CIRCUIT INFO
2
CIRCUIT INFO
(1 NET)
3
CALCULATE RECOMMENDED
CIRCUIT INFO
4
RECOMMENDED
CIRCUIT INFO
5
OUTPUT NOISE
COUNTERMEASURES
6
NOISE
COUNTERMEASURES
7
CREATE CIRCUIT MODEL
8
CIRCUIT SIMULATOR
9
NOISE CHECK
10
OPTIMIZE NOISE
COUNTERMEASURES
11
NOISE
COUNTERMEASURES
(AFTER OPTIMIZATION)

FIG. 5

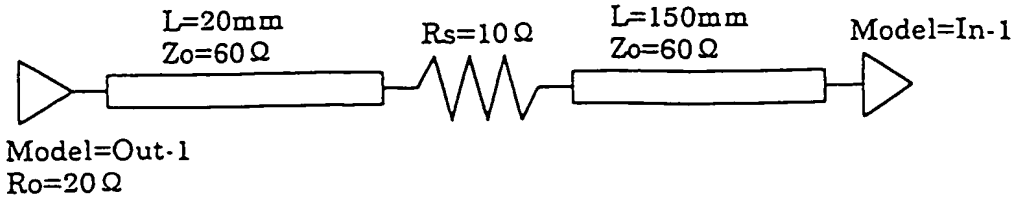

FIG. 6

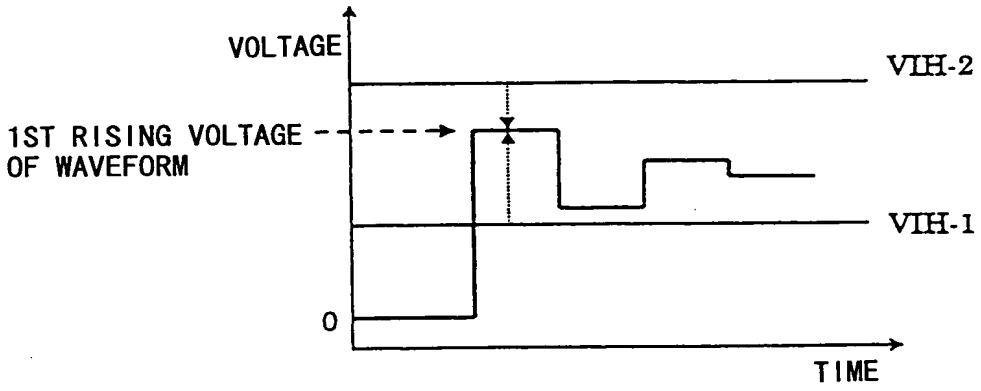

FIG. 7

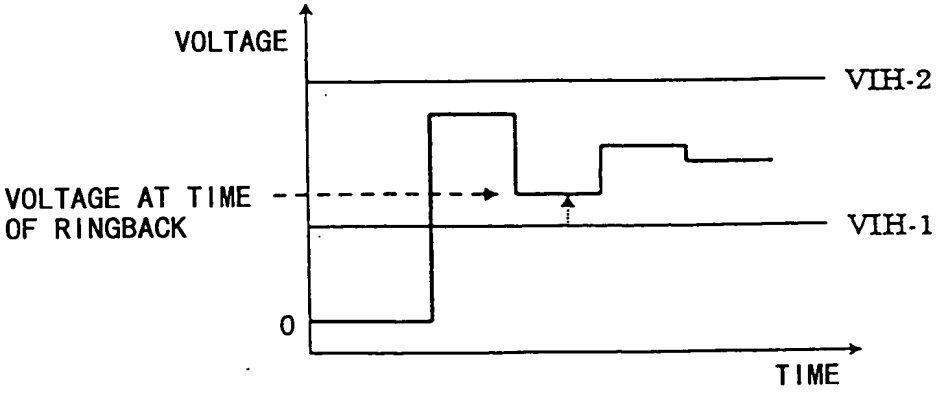

FIG.8

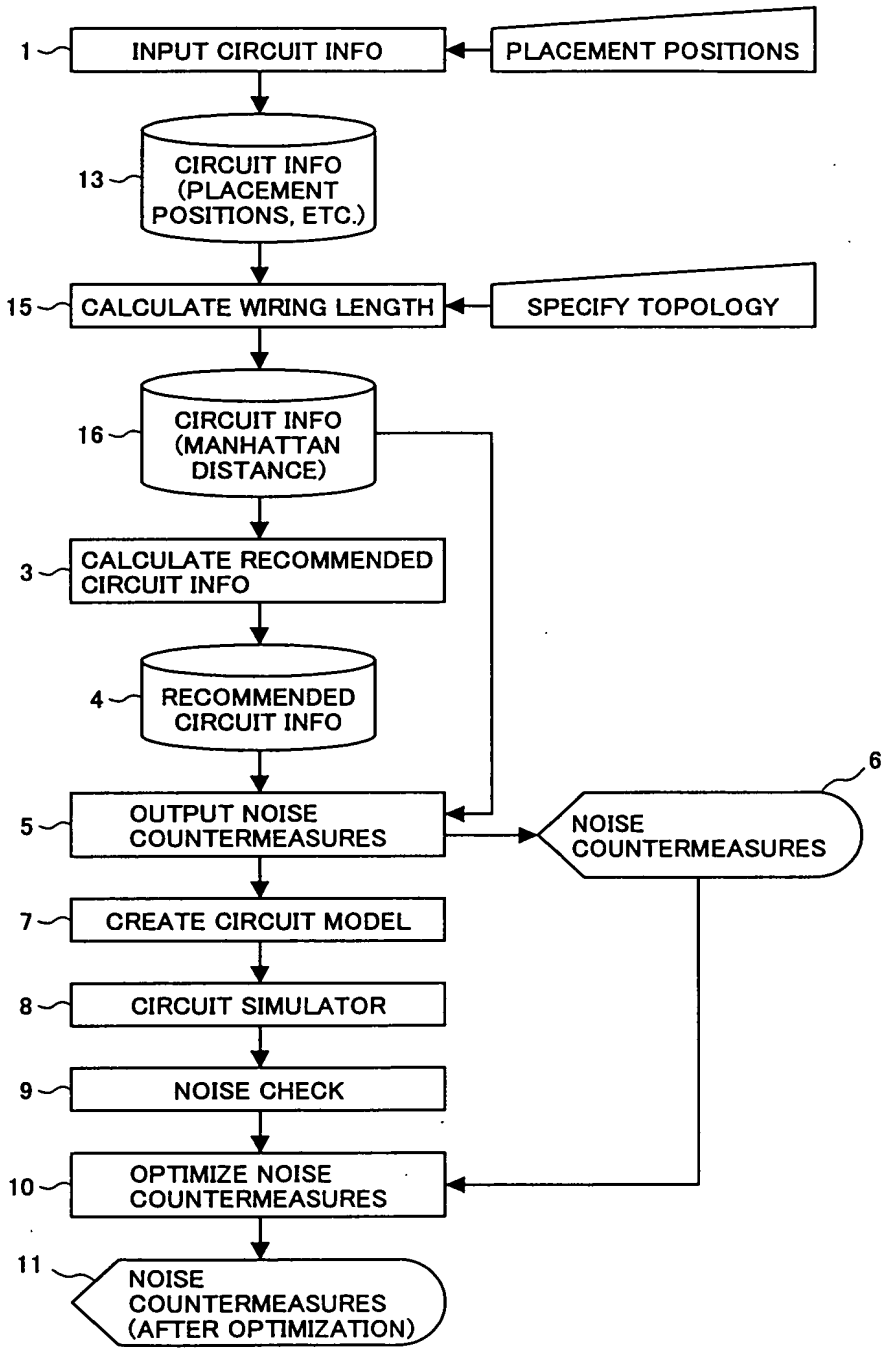
1
INPUT CIRCUIT INFO
PLACEMENT POSITIONS
13
CIRCUIT INFO (PLACEMENT POSITIONS, ETC.)
15
CALCULATE WIRING LENGTH
SPECIFY TOPOLOGY
16
CIRCUIT INFO (MANHATTAN DISTANCE)
3
CALCULATE RECOMMENDED CIRCUIT INFO
4
RECOMMENDED CIRCUIT INFO
6
5
OUTPUT NOISE COUNTERMEASURES
NOISE COUNTERMEASURES
7
CREATE CIRCUIT MODEL
8
CIRCUIT SIMULATOR
9
NOISE CHECK
10
OPTIMIZE NOISE COUNTERMEASURES
11
NOISE COUNTERMEASURES (AFTER OPTIMIZATION)

FIG. 9

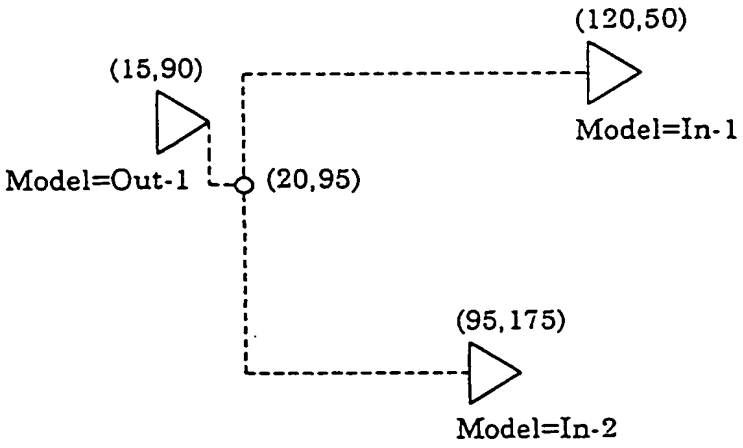

FIG.10

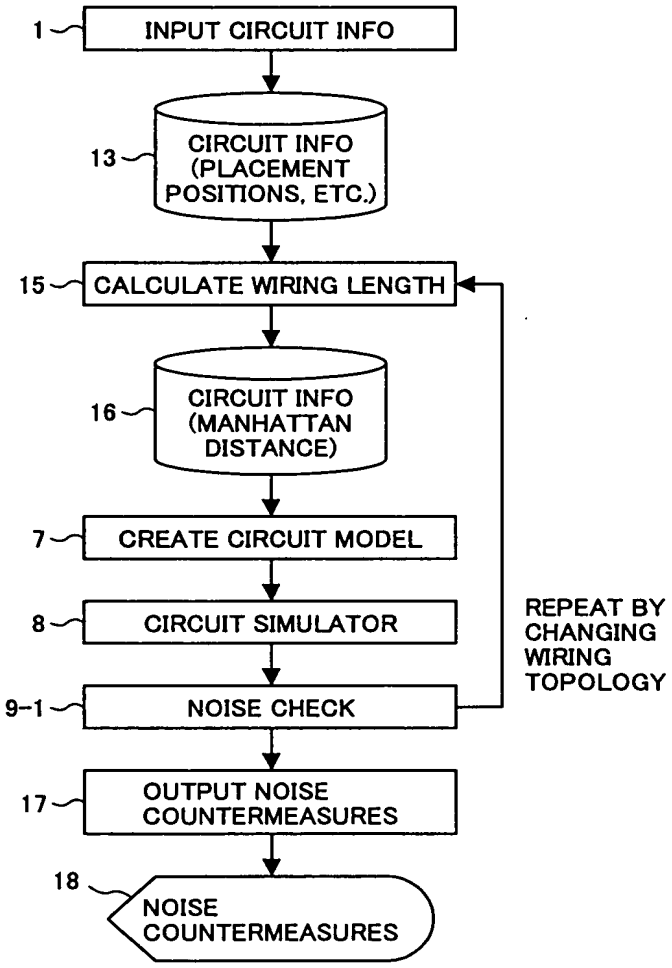
1
INPUT CIRCUIT INFO
13
CIRCUIT INFO (PLACEMENT POSITIONS, ETC.)
15
CALCULATE WIRING LENGTH
16
CIRCUIT INFO (MANHATTAN DISTANCE)
7
CREATE CIRCUIT MODEL
8
CIRCUIT SIMULATOR
9-1
NOISE CHECK
17
OUTPUT NOISE COUNTERMEASURES
18
NOISE COUNTERMEASURES
REPEAT BY CHANGING WIRING TOPOLOGY

FIG.11

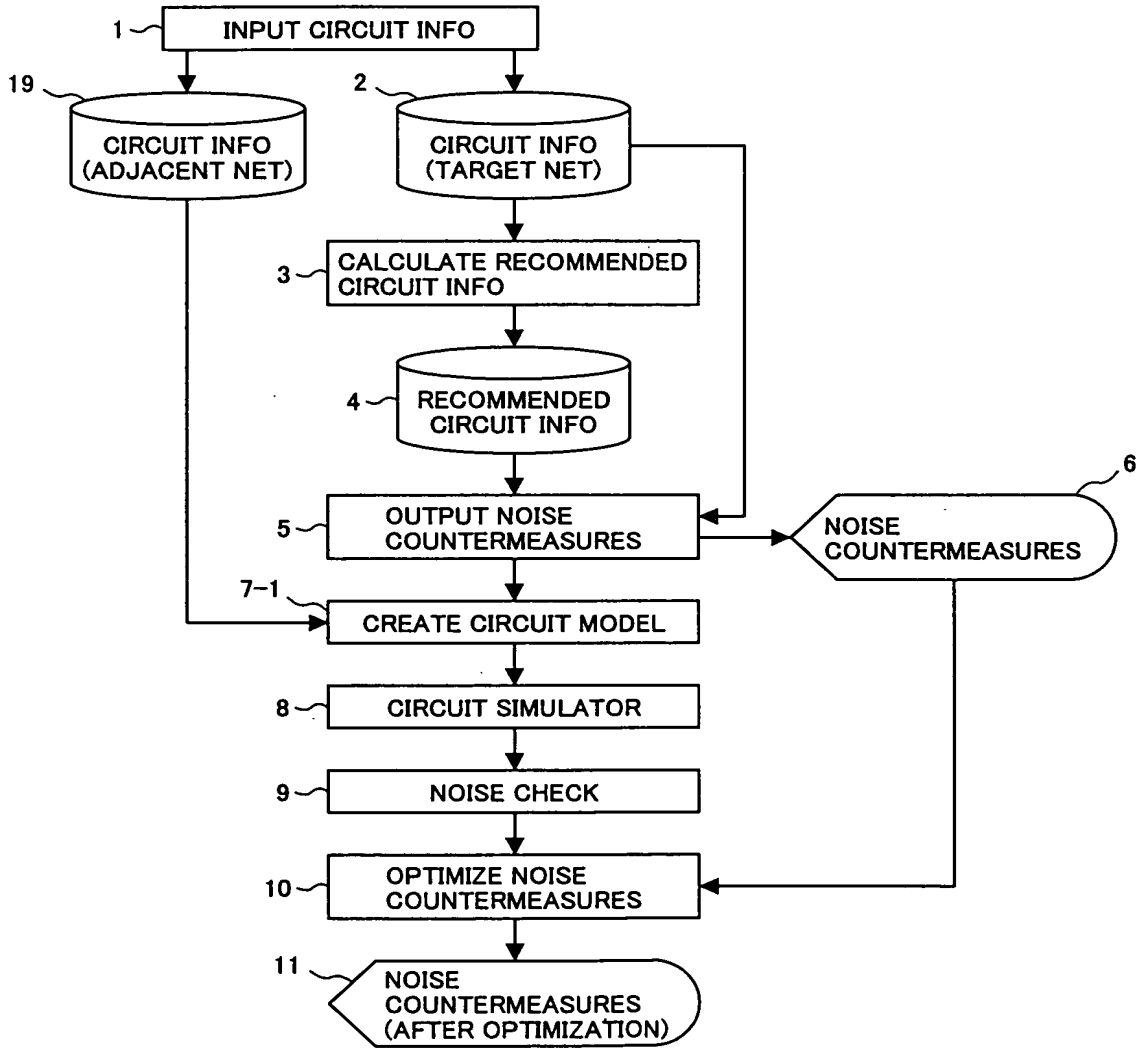
1
INPUT CIRCUIT INFO
19
CIRCUIT INFO (ADJACENT NET)
2
CIRCUIT INFO (TARGET NET)
3
CALCULATE RECOMMENDED CIRCUIT INFO
4
RECOMMENDED CIRCUIT INFO
5
OUTPUT NOISE COUNTERMEASURES
6
NOISE COUNTERMEASURES
7-1
CREATE CIRCUIT MODEL
8
CIRCUIT SIMULATOR
9
NOISE CHECK
10
OPTIMIZE NOISE COUNTERMEASURES
11
NOISE COUNTERMEASURES (AFTER OPTIMIZATION)

FIG. 12

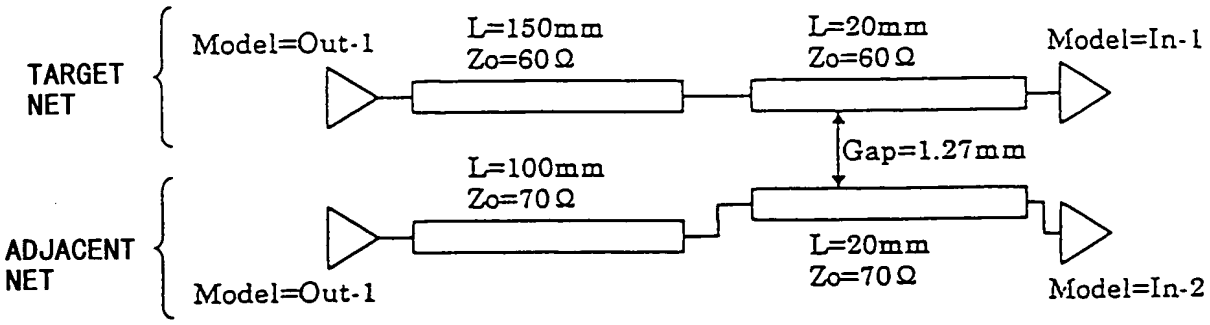
TARGET NET
Model=Out-1
L=150mm
Zo=60Ω
L=20mm
Zo=60Ω
Model=In-1
Gap=1.27mm
ADJACENT NET
L=100mm
Zo=70Ω
L=20mm
Zo=70Ω
Model=Out-1
Model=In-2

FIG.13

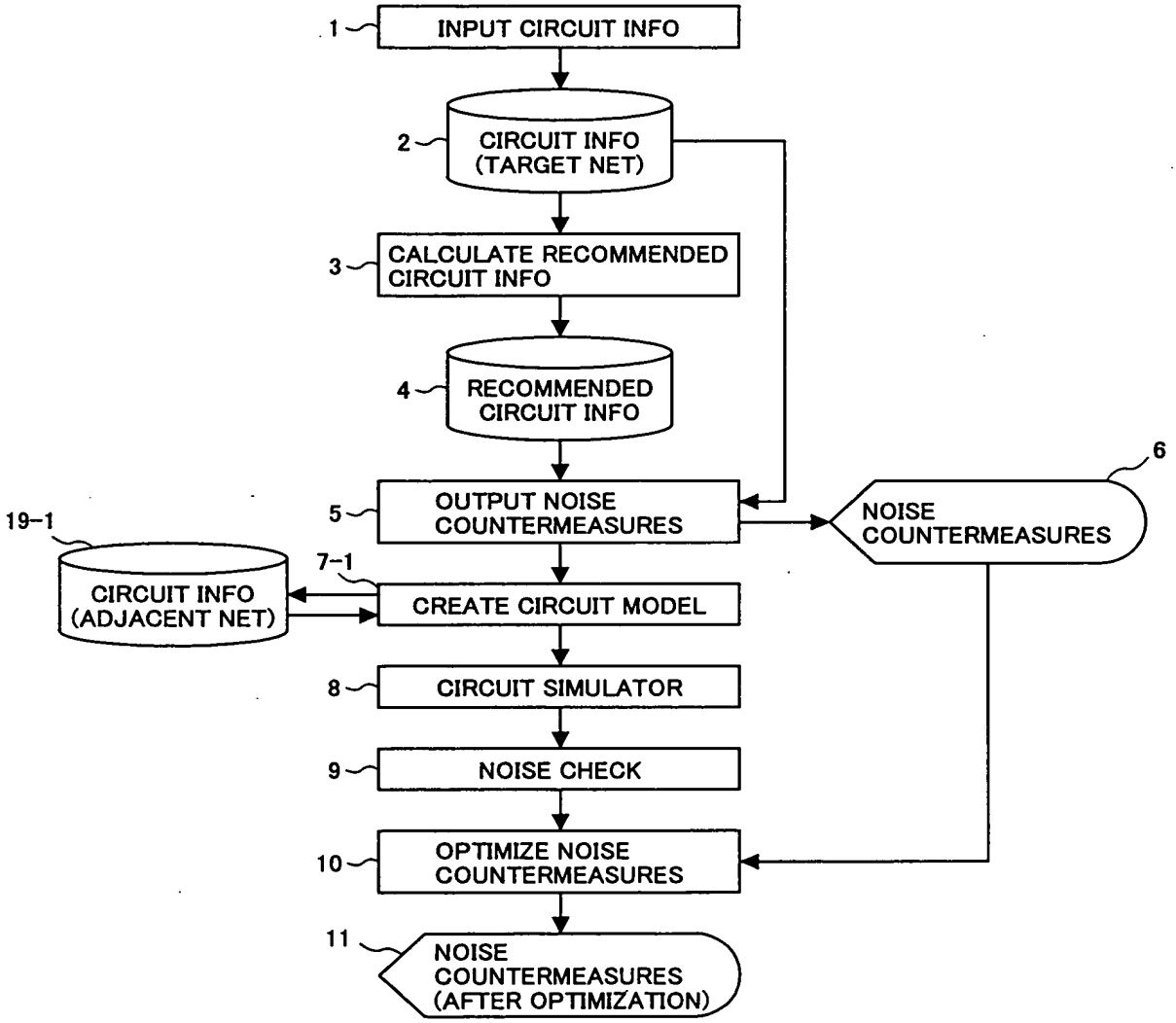
1
INPUT CIRCUIT INFO
2
CIRCUIT INFO (TARGET NET)
3
CALCULATE RECOMMENDED CIRCUIT INFO
4
RECOMMENDED CIRCUIT INFO
5
OUTPUT NOISE COUNTERMEASURES
6
NOISE COUNTERMEASURES
19-1
CIRCUIT INFO (ADJACENT NET)
7-1
CREATE CIRCUIT MODEL
8
CIRCUIT SIMULATOR
9
NOISE CHECK
10
OPTIMIZE NOISE COUNTERMEASURES
11
NOISE COUNTERMEASURES (AFTER OPTIMIZATION)

FIG. 14

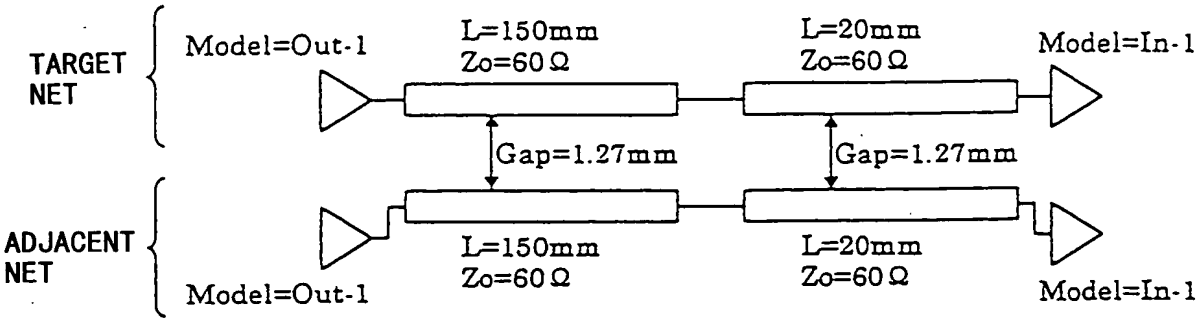
TARGET NET
Model=Out-1
L=150mm
Zo=60Ω
L=20mm
Zo=60Ω
Model=In-1
Gap=1.27mm
Gap=1.27mm
ADJACENT NET
L=150mm
Zo=60Ω
L=20mm
Zo=60Ω
Model=Out-1
Model=In-1

FIG.15

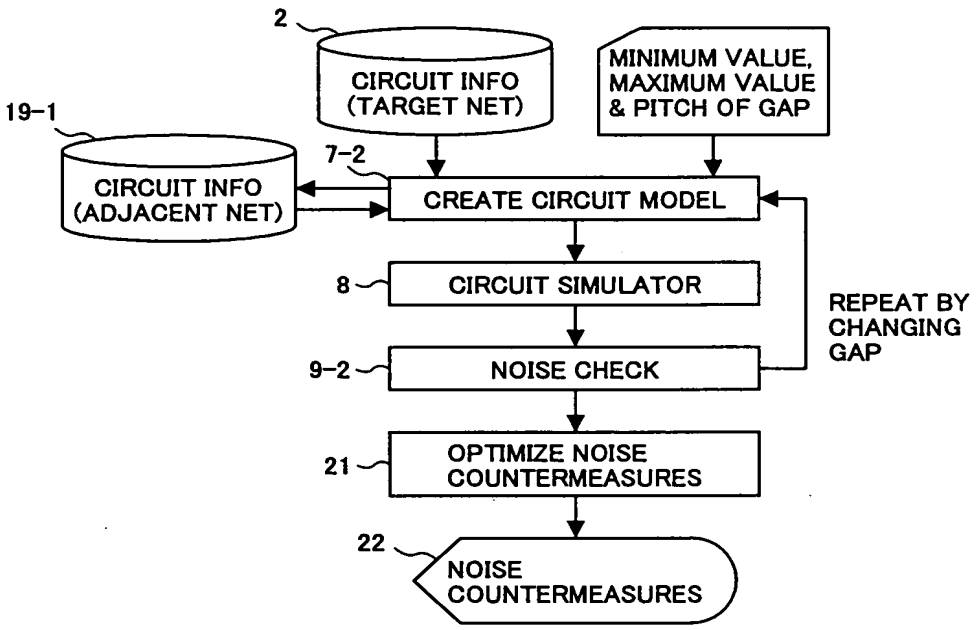
2
CIRCUIT INFO (TARGET NET)
MINIMUM VALUE, MAXIMUM VALUE & PITCH OF GAP
19-1
CIRCUIT INFO (ADJACENT NET)
7-2
CREATE CIRCUIT MODEL
8
CIRCUIT SIMULATOR
9-2
NOISE CHECK
REPEAT BY CHANGING GAP
21
OPTIMIZE NOISE COUNTERMEASURES
22
NOISE COUNTERMEASURES

FIG. 16

WIRING TOPOLOGY: LOAD CONCENTRATION TYPE
CHARACTERISTIC IMPEDANCE OF WIRING PATTERN: Z_0=60Ω
TRANSMISSION DELAY TIME OF WIRING PATTERN : T_d=7.0ns/m

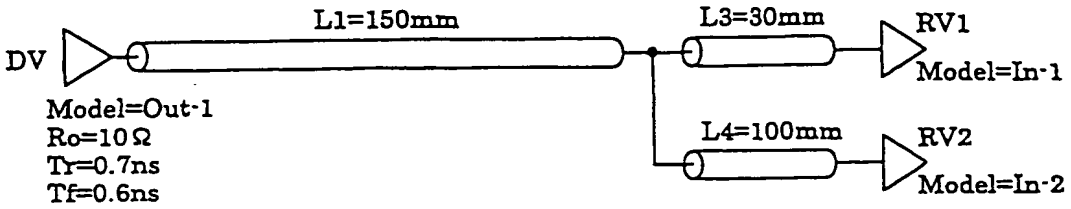

FIG. 17

WIRING TOPOLOGY: LOAD CONCENTRATION TYPE
CHARACTERISTIC IMPEDANCE OF WIRING PATTERN: Z_0=60Ω
TRANSMISSION DELAY TIME OF WIRING PATTERN : T_d=7.0ns/m

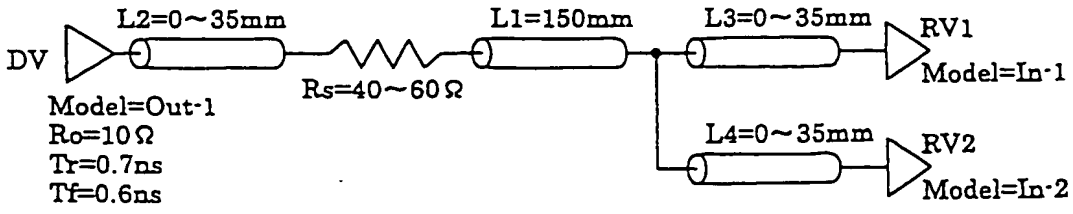

FIG. 18

WIRING TOPOLOGY: STAR TYPE
CHARACTERISTIC IMPEDANCE OF WIRING PATTERN: Z_0=60Ω
TRANSMISSION DELAY TIME OF WIRING PATTERN : T_d=7.0ns/m

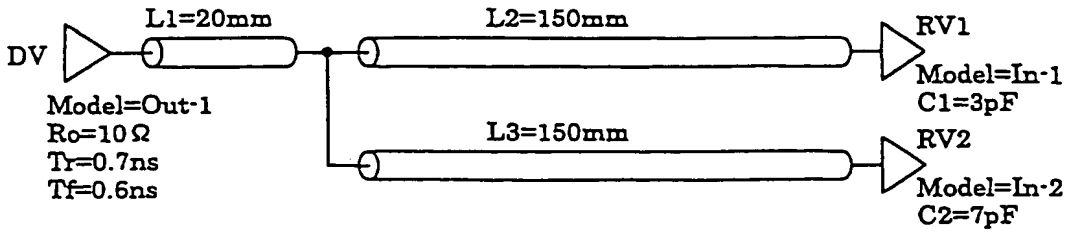

FIG. 19

WIRING TOPOLOGY: LOAD CONCENTRATION TYPE
CHARACTERISTIC IMPEDANCE OF WIRING PATTERN: Z_0=60Ω
TRANSMISSION DELAY TIME OF WIRING PATTERN : T_d=7.0ns/m

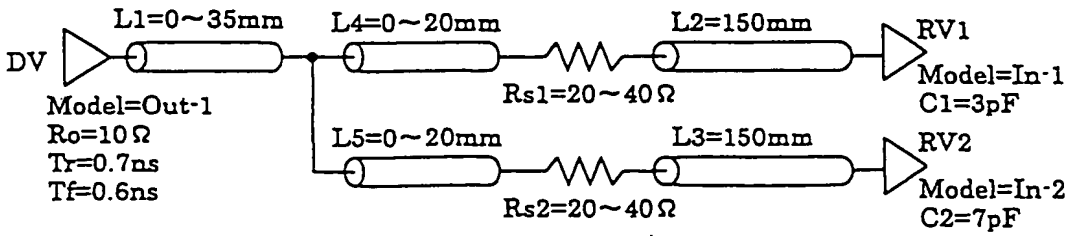

FIG. 20

WIRING TOPOLOGY: STAR TYPE
CHARACTERISTIC IMPEDANCE OF WIRING PATTERN: Z_0=60Ω
TRANSMISSION DELAY TIME OF WIRING PATTERN : T_d=7.0ns/m

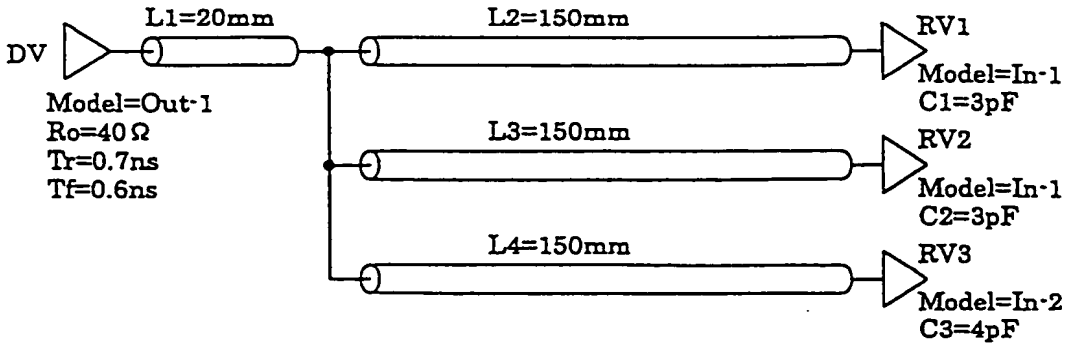

FIG. 21

WIRING TOPOLOGY: LOAD CONCENTRATION TYPE
CHARACTERISTIC IMPEDANCE OF WIRING PATTERN: Z_0=60Ω
TRANSMISSION DELAY TIME OF WIRING PATTERN : T_d=7.0ns/m

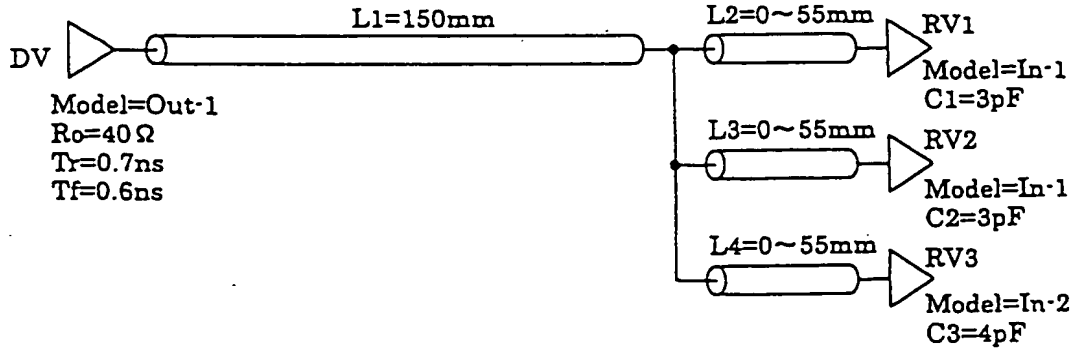

FIG.22

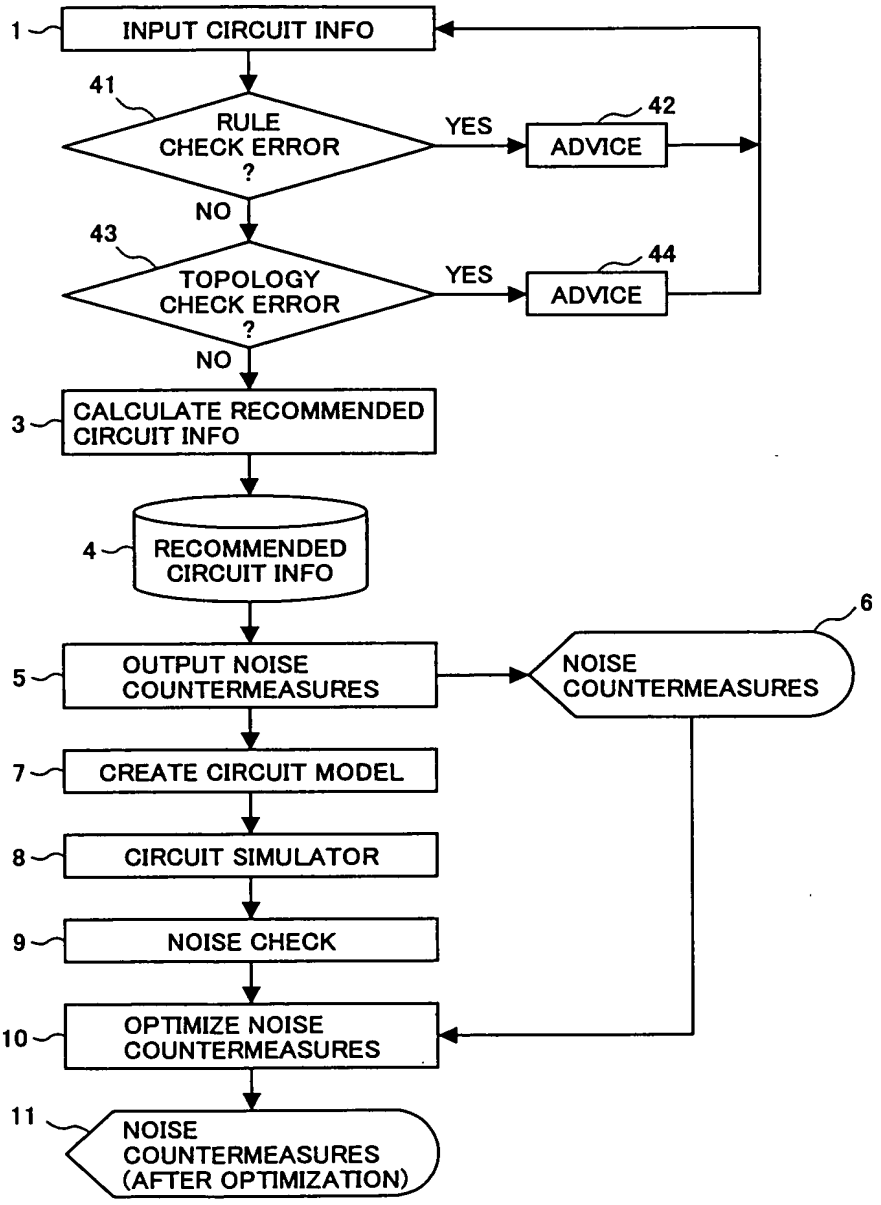
1
INPUT CIRCUIT INFO
41
RULE CHECK ERROR ?
YES
42
ADVICE
NO
43
TOPOLOGY CHECK ERROR ?
YES
44
ADVICE
NO
3
CALCULATE RECOMMENDED CIRCUIT INFO
4
RECOMMENDED CIRCUIT INFO
5
OUTPUT NOISE COUNTERMEASURES
6
NOISE COUNTERMEASURES
7
CREATE CIRCUIT MODEL
8
CIRCUIT SIMULATOR
9
NOISE CHECK
10
OPTIMIZE NOISE COUNTERMEASURES
11
NOISE COUNTERMEASURES (AFTER OPTIMIZATION)

FIG.23

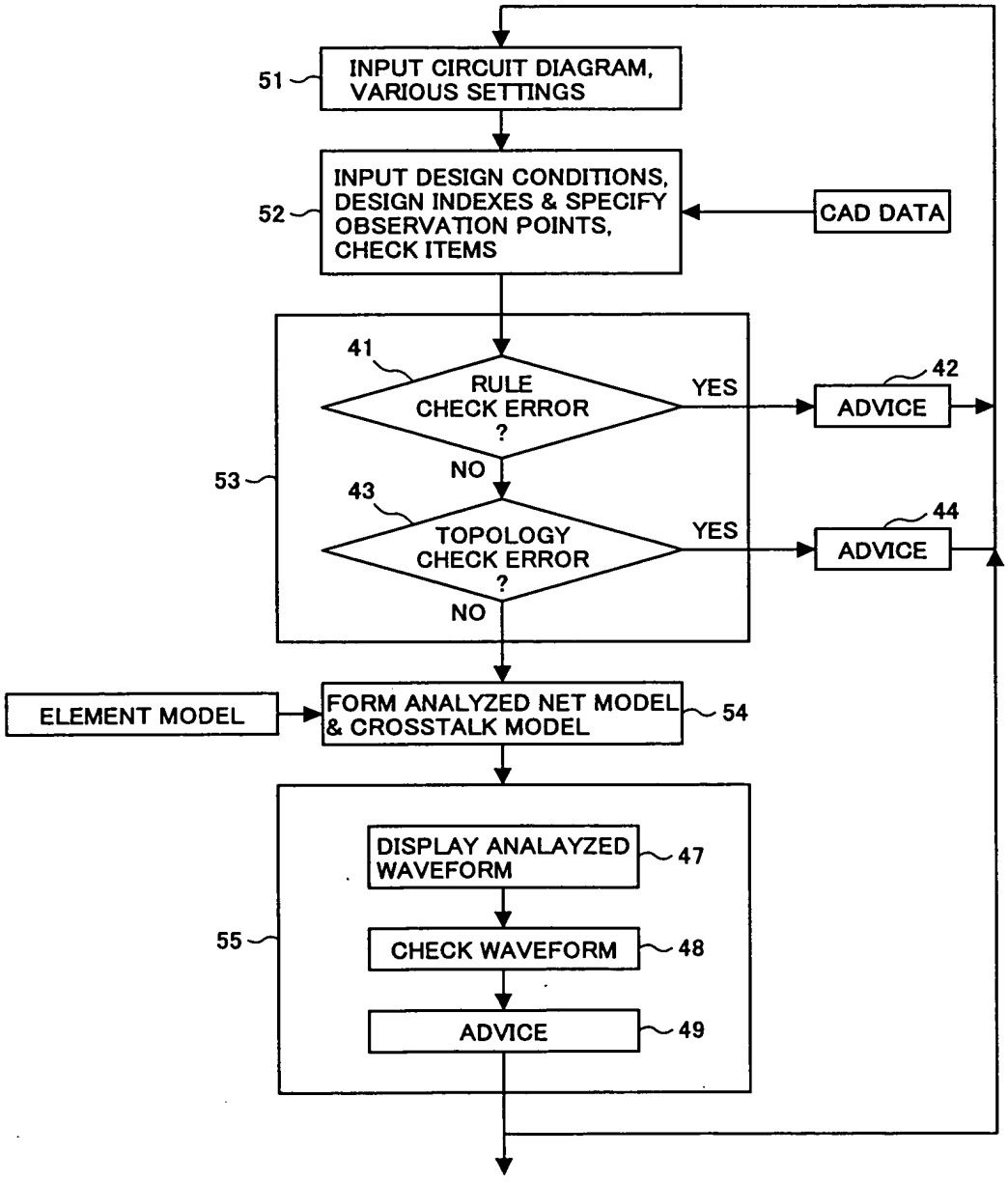
51
INPUT CIRCUIT DIAGRAM, VARIOUS SETTINGS
52
INPUT DESIGN CONDITIONS, DESIGN INDEXES & SPECIFY OBSERVATION POINTS, CHECK ITEMS
CAD DATA
53
41
RULE CHECK ERROR ?
YES
42
ADVICE
NO
43
TOPOLOGY CHECK ERROR ?
YES
44
ADVICE
NO
ELEMENT MODEL
FORM ANALYZED NET MODEL & CROSSTALK MODEL
54
55
DISPLAY ANALAYZED WAVEFORM
47
CHECK WAVEFORM
48
ADVICE
49

FIG. 24

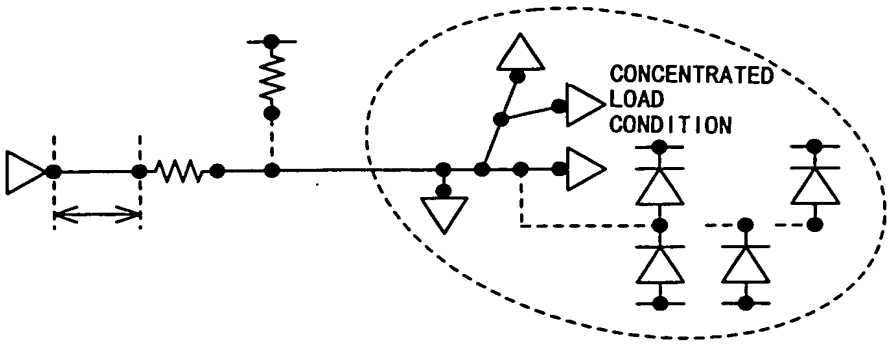

FIG. 25A

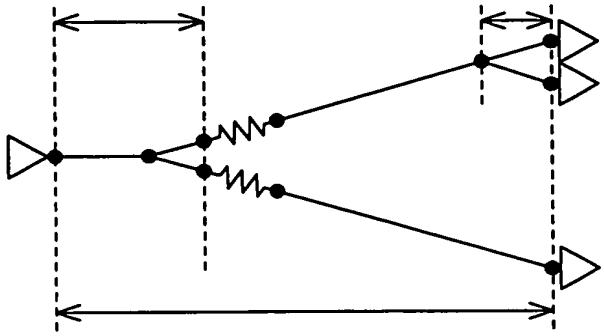

FIG. 25B

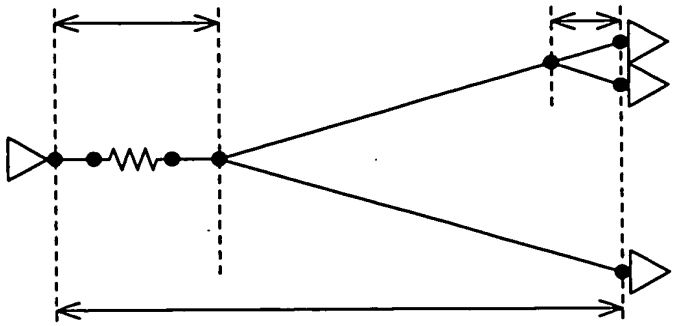

FIG. 26A

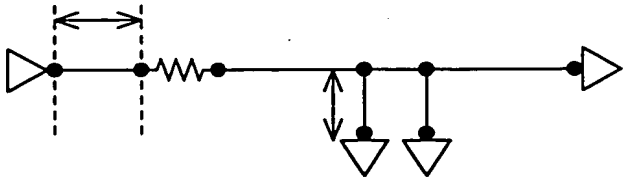

FIG. 26B